

Chapter 38

An All-Inversion-Region g_m/I_D Based Design Methodology for Radiofrequency Blocks in CMOS Nanometer Technologies

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ABSTRACT

This chapter presents a design optimization methodology for analog radiofrequency (RF) blocks based on the g_m/I_D technique and on the exploration of all-inversion regions (from weak inversion or sub-threshold to strong inversion or above threshold) of the MOS transistor in nanometer technologies. The use of semi-empirical models of MOS transistors and passive components, as inductors or capacitors, assures accurate designs, reducing time and efforts for transferring the initial block specifications to a compliant design. This methodology permits the generation of graphical maps to visualize the evolution of the circuit characteristics when sweeping both the inversion zone and the bias current, allowing reaching very good compromises between performance aspects of the circuit (e.g. noise and power consumption) for a set of initial specifications. In order to demonstrate the effectiveness of this methodology, it is applied in the design of two basic blocks of RF transceivers: low noise amplifiers (LNAs) and voltage controlled oscillators (VCOs), implemented in two different nanometer technologies and specified to be part of a 2.4 GHz transceiver. A possible design flow of each block is provided; resulting designs are implemented and verified both with simulations and measurements.

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INTRODUCTION

The variety of wireless applications in areas as diverse as medicine, entertainment or environment have originated a wide spectrum of wireless standards and therefore, of circuit specifications. This diversity in the circuit characteristics together with the shrinking time to market results in design challenges. To keep pace with this innovation, RF designers, as never before, need reliable optimization tools helping them from the beginning of the design process.

Some RF standards are very demanding in terms of power consumption but they have relaxed performance requirements e.g. in terms of channel bandwidth or noise and frequency synthesizer spectral purity, as in the case of IEEE 802.15.4 standard (on which ZigBee is based) and low-energy Bluetooth (IEEE 802.15.1-2002). Power consumption constrains the transceiver design and forces to assign carefully the power budget of each block of the chain. It also has a strong influence on the noise, linearity, gain and other characteristics. A well known trade-off is especially noticeable between power and inherent noise of blocks as LNAs, mixers or VCOs. To take advantage of this compromise, the designer needs a deep and accurate knowledge of the block behavior and its devices to reach an optimized design, especially when using nanometer technologies.

The trade-offs between consumption and noise, among other performances, are strongly determined by the characteristics of the active element: the MOS transistor. These characteristics change as a function of the inversion region in which the MOS transistor is biased: strong inversion (above threshold), moderate inversion (approximately “around” threshold) and weak inversion (sub-threshold). In the following section a summary of the characteristics and the implications of working in each of these zones are presented.

When working in radiofrequency, the MOS transistor has been traditionally biased in strong inversion. It is because in this region the transis-

tor has a smaller size and drives a higher current than in moderate or weak inversion. This leads to a reduction of parasitic capacitances and an increment in the transconductance. Therefore, as the MOS transition frequency f_T is proportional to the transconductance and to the inverse of its parasitic capacitance, the maximum frequency of operation increases in strong inversion region. However, as it will be shown later, this increased maximum frequency of operation is obtained at the expense of a very low ratio between transconductance and bias current (below 5 V^{-1} instead of the 38 V^{-1} achievable with a bipolar transistor at ambient temperature). The effect of moving from strong inversion through weak inversion implied a considerable current reduction, but in contrast, parasitic capacitances are higher as transistor dimensions increase. For example, for sub-micrometer technologies the high frequency design in moderate was limited up to one gigahertz (Barboni, Fiorelli & Silveira, 2006).

However, the tremendous channel length reduction to below 100 nm, and the improvement in passive components, i.e. inductors and capacitors, are opening the path to feasible implementations. So, nowadays it is possible to use CMOS technology without increasing the consumption and even reduce it much more by working in the moderate and weak inversion in the range of several gigahertz for minimum length transistor. This can be achieved even considering the MOS transistor working above the quasi-static limit of one tenth of f_T (Tsividis, 2000, p. 492) and therefore greatly simplifying the circuit analysis.

Many implementation examples working in moderate and weak inversion are found in literature. Porret, Melly, Python, Enz and Vittoz (2001) and Melly, Porret, Enz, and Vittoz (2001) presented the design of a receiver and a transmitter, respectively, for 433 MHz in CMOS, working in moderate inversion. Ramos et al. (2004) showed the design of an LNA in 90 nm technology for 900 MHz in moderate/weak inversion. Barboni et al. (2006) utilized the moderate inversion to implement an

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