Chapter 90
Random Dynamical Network Automata for Nanoelectronics:
A Robustness and Learning Perspective[1]

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ABSTRACT

It is generally expected that future and emerging nanoscale computing devices will be built in a bottom-up way from vast numbers of simple, densely arranged components that exhibit high failure rates, are relatively slow, and connected in an unstructured way. Other than that, there is little to no consensus on what type of technology and computing architecture holds most promises to go far beyond today's top-down engineered silicon devices. Highly structured crossbar-like and cellular automata architectures have been proposed as possible alternatives to the von Neumann computing architecture, which is not generally well suited for emerging, massively parallel and fine-grained nanoscale electronics. While the top-down engineered semi-conducting technology favors regular and locally interconnected structures, emerging bottom-up self-assembled devices tend to have to be unstructured and heterogeneous because of the current lack of precise control over these processes. In this paper, we survey and assess two types of random dynamical networks, namely Random Boolean Networks (RBNs) and Random Threshold Networks (RTNs), as candidates for alternative computing architectures and models for future nanoscale information processing devices. In a high-level approach that is based on previous work, we illustrate that they have the potential to offer superior properties over highly structured crossbar- or mesh-like cellular automata architectures, such as an inherent and scale-invariant robustness, more efficient communication capabilities, manufacturing benefits for bottom-up self-assembled devices, and the ability to learn and solve tasks successfully. We also show that RBNs can learn and generalize. Our investigation is driven by the need for alternative computing and manufacturing paradigms to mitigate some of the challenges traditional approaches face.

INTRODUCTION AND MOTIVATION

The advent of multicore architectures and the slowdown of the processor's operating frequency increase are signs that CMOS miniaturization is increasingly hitting fundamental physical limits. A key question the industry faces is how computing architectures will evolve as we reach these fundamental limits. What type of device and architecture will guarantee a sustainable and continuous progress in the information and communication technology for the next 10-20 years? A likely possibility within the realm of CMOS technology is that the integration density will cease to increase at some point, instead, only the number of components, i.e, the number of transistors, will continue to increase, which will lead to chips with a higher area. This trend can be observed with current multi-core architectures, and is expected to continue. Besides the unsolved challenge of programming large multi-core systems, the trend has implications on the interconnect architecture, the power consumption and heat dissipation, and the reliability. Another possibility lies in the smooth and incremental transition to hybrid systems, which combine traditional silicon technology with new nano- and molecular-scale components, such as carbon nanotubes and nanowires. Yet another possibility is to go beyond silicon-based technology and to radically change the computing and manufacturing paradigms, by using for example bottom-up self-assembled devices. Self-assembling nanowires (Ferry, 2008) or carbon nanotube electronics (Avouris, Chen, & Perebeinos, 2007) are promising candidates, although none of them has resulted in electronics that is able to compete with traditional CMOS so far. What seems clear is that the current way with build computers and the way we algorithmically solve problems with them may need to be fundamentally revisited. The goal of this paper is to explore such a radical new approach and to evaluate its potential.

While the top-down engineered CMOS technology favors regular and locally interconnected structures, future bottom-up self-assembled devices tend to have irregular structures because of the current lack of precise control over these processes. We therefore hypothesize that, compared to current CMOS technology, which allowed engineers to implement a logic-based computing architecture with extreme precision and reliability, future and emerging computing architectures will be increasingly driven by manufacturing constraints and particularities. Independent of the emerging device and fabrication technologies, we assume in this paper that future nanoscale devices will be built from (1) vast numbers of densely arranged devices that (2) are arranged and interconnected in some unstructured way and that (3) exhibit high failure rates. We take this working hypothesis for granted in this paper and address it from a perspective that focuses on the interconnect topology. This is justified by the fact that the importance of interconnects on electronic chips has outrun the importance of transistors as a dominant factor of performance (Meindl, 2003; Ho, Mai, & Horowitz, 2001; Davis et al., 2001). The reasons for that are twofold: (1) the transistor switching speed for traditional silicon is much faster than the average wire delays and (2) the required chip area for interconnects has increased.

In (Zhirnov, Cavin, Leeming, & Galatsis, 2008), Zhirnov et al. explored integrated digital *Cellular Automata* (CA) architectures—which are highly regular structures with local interconnects (see Section)—as an alternative paradigm to the von Neumann computer architecture for future and emerging information processing devices. They argue that CAs are well suited for semiconductor technology, which "[…] favors the realization of regular, locally connected structures […]." Here, we are interested to explore and assess a more general class of discrete dynamical systems, namely *Random Boolean Networks* (RBNs) and *Random Threshold Networks* (RTNs), for emerging technologies. We will focus on RBNs, but RTNs are included in this paper because they offer an alternative paradigm to Boolean logic,

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