

Chapter 64

Built-In Self Repair for Logic Structures

Tobias Koal

Brandenburg University of Technology Cottbus, Germany

Heinrich T. Vierhaus

Brandenburg University of Technology Cottbus, Germany

ABSTRACT

For several years, many authors have predicted that nano-scale integrated devices and circuits will have a rising sensitivity to both transient and permanent faults effects. Essentially, there seems to be an emerging demand for building highly dependable hardware/software systems from unreliable components. Most of the effort has so far gone into the detection and compensation of transient fault effects. More recently, also the possibility of repairing permanent faults, due to either production flaws or to wear-out effects after some time of operation in the field of application, needs further investigation. While built-in self test (BIST) and even self repair (BISR) for regular structures such as static memories (SRAMs) is well understood, concepts for in-system repair of irregular logic and interconnects are few and mainly based on field-programmable gate-arrays (FPGAs) as the basic implementation. In this chapter, the authors try to analyse different schemes of logic (self-) repair with respect to cost and limitations, using repair schemes that are not based on FPGAs. It can be shown that such schemes are feasible, but need lot of attention in terms of hidden single points of failure.

INTRODUCTION

There are new fault mechanisms in nano-scale integrated circuits which tend to result in wear-out effects. Such effects essentially limit the life-time design of integrated systems in a way that has not

been seen before. For systems that have to work in safety-critical applications and, more generally, for systems that have to give a dependable service over a time of many years, the control and the eventual repair of such faults is becoming an essential issue in system design technology. The essential task then is to design systems in such a way that they can work with a high degree of

DOI: 10.4018/978-1-4666-5125-8.ch064

dependability, even if some of their essential basic components such as metal lines, transistors, and insulation layers are not highly reliable. This is a new challenge to integrated circuit and systems design technology, since in the past the overall system life time in entities such as personal computers was mainly limited not by integrated sub-systems, but by other devices such as capacitors and power supply units. This chapter first gives an overview over recent developments concerning new fault mechanism in nano-electronics and their possible implications. Then it introduces basic technologies of built-in self repair (BISR). After a discussion of reconfiguration and repair based on FPGA structures, other schemes that may work on standard CMOS logic are introduced. The chapter then discusses overheads and limitations of different architectures. Finally, the reader is sensitized to take care of “single points of failure” even in system designs that look highly reliable at the first glance.

BACKGROUND

Problems with embedded electronic systems in safety-critical application are not new. For example, European car-makers lagged behind Japanese manufacturers for years in the break-down statistics of automobile clubs, mainly because of problems in electronic sub-systems. This has changed recently due to intensive efforts and high investments from the European automotive industry. While problems of software validation have been a matter of concern for a long time, hardware was often considered to be more reliable, with the possible exception of contacts, plugs and sockets. Apparently, this situation has been changing with the arrival of semiconductor technologies that use nano-structures.

For several years authors have predicted upcoming problems with integrated nano-scale technologies (Sirisantana, S., Paul, B. C. & Roy, K., 2004, Mishra, M. Goldstein, S.C., 2003,

Breuer, M. L., Gupta, S. K. & Mak, T. M., 2004, Abraham, J., 2008, Kopetz, A., 2008). Some of the effects have been known for some time, such as single event upsets (SEUs) and even multi-event upsets (MEUs), mainly in flip-flops, latches and memory devices (Baumann, R., 2005, Seifert, M. & Tam, N., 2004, Mitra, S., Seifert, N., Zhang, M., Shi, Q. & Kim, K. S., 2005. These transient faults are mainly due to charged particles and electromagnetic coupling, and they cause malfunctions, mostly without leaving a permanent damage. Such mechanisms are dealt with in detail in chapter 2-1 of this book. Essentially, transient fault effects can be dealt with by well established methods and architectures of fault-tolerant computing (Pradhan, D., 1996, Gössel, M., Ocheretny, V., Sogomonyan, E. & Marienfeld, D., 2008). In this area, the focus of recent research is on double- and multiple bit faults, due to the rising danger of multiple-bit upsets (Richter, M. & Gössel, M., 2009). However, there are also new mechanisms for permanent defects that may harm production yield and long-time circuit reliability (Borkar, S., 2005, Cao, Y., Bose, P. & Tschanz, J., 2009, Abella, J., Vera, X., Unsal, O., Ergin, O., Gonzalez, A. & Tschanz, J., 2008, Fang, P., Tao, J., Chen, J. F. & Hu, C., 1998). For parameter flaws and defects that have a direct impact on production yield, mapping and alignment problems in deep-UV-lithography play a major role. Also statistical variations in the channel doping distribution of single MOS transistors may become critical, since such variations have a direct impact on the transistor threshold voltage V_{th} . If the V_{th} value is much below the nominal value, the transistor will be “always on” or allow for high leakage currents, while a too-high V_{th} value makes transistors with poor switching properties or even an “always-off” behaviour. While traditional ICs, produced with minimum feature size of 200 nano-meters and above, seem to have a very long life time with little deterioration of parameters, nano-circuits carry a much higher risk. Problems arise from high current density on thin metal lines and subsequent metal migra-

25 more pages are available in the full version of this document, which may be purchased using the "Add to Cart" button on the publisher's webpage:
www.igi-global.com/chapter/built-in-self-repair-for-logic-structures/102074

Related Content

Nanotechnology Innovation Systems: A Regional Comparison

Nazrul Islam (2010). *International Journal of Nanotechnology and Molecular Computation* (pp. 65-84).
www.irma-international.org/article/nanotechnology-innovation-systems/48529

Guiding the Next Technological Revolution: Principles for Responsible AI and Nanotech Progress

Ray Gutierrez Jr. (2024). *Artificial Intelligence in the Age of Nanotechnology* (pp. 210-232).
www.irma-international.org/chapter/guiding-the-next-technological-revolution/334941

Exploring Novel Strategies for Lipid-Based Drug Delivery

Sabna Kotta, Navneet Sharma, Prateek Raturi, Mohd Aleem and Rakesh Kumar Sharma (2018). *Journal of Nanotoxicology and Nanomedicine* (pp. 1-22).
www.irma-international.org/article/exploring-novel-strategies-for-lipid-based-drug-delivery/227426

Quantum Backpropagation Neural Network Approach for Modeling of Phenol Adsorption from Aqueous Solution by Orange Peel Ash

Siddhartha Bhattacharjee, Siddhartha Bhattacharyya and Naba Kumar Mondal (2014). *Nanotechnology: Concepts, Methodologies, Tools, and Applications* (pp. 1254-1275).
www.irma-international.org/chapter/quantum-backpropagation-neural-network-approach-for-modeling-of-phenol-adsorption-from-aqueous-solution-by-orange-peel-ash/102066

An Assessment of Random Dynamical Network Automata for Nanoelectronics

Christof Teuscher, Natali Gulbahce and Thimo Rohlf (2009). *International Journal of Nanotechnology and Molecular Computation* (pp. 58-76).
www.irma-international.org/article/assessment-random-dynamical-network-automata/40365