Chapter 5
CNTFET-Based Ternary Logic Gates:
Design and Analysis Approach

Suman Rani
I.K.G. Punjab Technical University Jalandhar, Punjab, India & Baba Farid College of Engineering and Technology, Bathinda, India.

Balwinder Singh
ACS Division, Centre for Development of Advanced Computing, Mohali, India

ABSTRACT

In the recent digital designs, there are certain circumstances where energy efficiency and ease is required, and in such situations, ternary logic (or three-valued logic) is favored. Ternary logic is an auspicious supernumerary to the conventional binary (0, 1) logic design techniques as this one is possible to attain straightforwardness and energy efficiency. This chapter deals with the comparative analysis of CMOS and CNTFET-based ternary inverter and universal gates design. The simulation result is analyzed and validated with a Hailey simulation program with integrated circuit (HSPICE) simulations. The average delay and power consumption in CNTFET-based ternary inverter have been reduced by approximately 90.3% and 48.8% respectively, as compared to CMOS-based ternary inverter design. Likewise, delay is reduced by 50% and power gets 99% reduction in ternary CNTFET NAND gate as compared to CMOS-based ternary NAND gat. It is concluded that CNFETs are faster and consume less power compared to CMOS technology.

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1. INTRODUCTION

Simplicity and energy efficiency are one of the most significant features of up-to-date electronics systems intended for high-performance handy applications. Usually, Logics and algorithms in digital computations are based on the two-valued code, that is, high or low, or yes or no or (0 or 1). On the other hand, in few conditions, we exercise a state in which it is problematic otherwise needless to choose right or false. For illustration, in a transient state (changes from 0 to 1 or 1 to 0), it is difficult to resolve whether the value of the state is 0 or 1. Then ternary logic (three-valued logic) can be used, as an alternative of binary logic (two-valued logic), in which the third value i.e truth is familiarized to signify an indefinite state separately since true and false. Henceforth multivalued Logic substitutes the conventional Boolean characterization of the variable by many values for example Ternary logic (Mukaidono, 1986, p.179).

One of the utmost common MVL areas is Łukasiewicz (1970) and Kleene (1954). Out of these two most predominant MVL fields, Kleene field has been extra widespread and suitable owing to its representative nature and suitable definition for basic operators in the computer discipline world (Azhari et al., 2015). Surrounded by all MVL systems, with e base (e=2.718) principals to the furthermost well-organized implementation of the switching systems. Meanwhile 3 is the nearby amount to e, ternary logic is the superlative substitute for designing the MVL circuits (Moaiyeri et al., 2011, p. 285). Ternary logic offers numerous important benefits over the binary logic in digital designs. For illustration, extra information can be transferred over a specified set of lines, interconnections complexity can be reduced and reduction in components count can be achieved. Moreover, serial and serial-parallel arithmetic actions can be passed faster if three-valued logic is engaged (Balla & Antoniou, 1984, p. 739). Broad investigation on the design and implementation of ternary logic with depletion enhancement complementary metal-oxide-semiconductor (DE-CMOS) integrated circuits can be originatein the technical literature (Heung & Mouftah, 1985, p. 609). Based on MOS technology MVL circuits further categories as Current-mode MVL circuits and another one is Voltage-mode MVL circuits. Owing to the ballistic conduction (high performance) and low I_{OFF} (low power consumption) belongings of Carbon Nanotube Field-effect transistors (CNTFETs) are an appropriate choice toward the buck silicon transistors for the design of logic circuits. The CMOS based multi-threshold design depends on the body effects with changed bias voltages to the base terminal of the transistors (Kumar et al., 2019, p. 3). But in event of the CNTFET based multi-threshold design, the diameter (D) of the CNT determines the threshold voltage (V_{TH}) of the transistor. Thus, a multi-threshold design can be consummate through CNTs with altered diameters in the CNTFETs. Novel techniques based on CNTFET used for