Chapter 6
Low Power, High Performance CNTFET-Based SRAM Cell Designs:
Design and Analysis of 6T CNTFET SRAM Cells

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ABSTRACT

The main objective of this chapter is to provide high-performance, low-power solutions for VLSI system designers. As technology scales down to 32nm and below, the present CMOS technology has to face the scaling limit, such as the increased leakage power, SCEs, and so on. To overcome these limits, the researchers have experimented on other technologies, among which a CNT technology-based device called CNTFET has been evaluated as one of the promising replacements to CMOS technology. In any digital systems, memory is an integral part, and it is also the largest constituent. SRAM is a widely used memory. In today's ICs, SRAM is going to occupy 60-70% of the total chip area. In this connection, this chapter describes the design of CNTFET-based 6T SRAM cell using circuit-level leakage reduction techniques, named sleep transistor, forced stack, data-retention sleep transistor, and stacked sleep.

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1. MOTIVATION

Previously, the prime objectives of the VLSI designer were area, performance, cost and reliability, but power consideration was mostly of only secondary importance. In the present scenario the power consumption became a major concern. Continuous decrease in the feature size and the consequent increase in chip density and operating frequency have made power consumption a major concern in VLSI design (Meindl, 1995).

For a CMOS circuit, the total power dissipation consists of dynamic power and static power. In the standby mode, the power dissipation is due to the leakage current. Dynamic power has two components, called short circuit power and switching power. One is due to charging and discharging of load capacitance called the switching power. The other is due to the non-zero rise and fall time of input waveforms called short circuit power. Leakage power is the consumed power that is due to the current flowing through the transistors of a circuit that are in the cut-off state.

Reduction of supply voltage reduces the power dissipation; this is because the power dissipation has quadratic relationship with the supply voltage. But reducing the supply voltage degrades the performance. In order to satisfy the high performance requirements, V_{TH} has to be scaled. Unfortunately, such scaling leads to a dramatic increase in leakage current, which becomes a new concern for low power and high performance circuit designs (Chandrakasan, Sheng & Brodersen, 1992). Earlier in micrometer technologies the dynamic power is the predominant component of the total power but in nanometer technologies leakage power is the dominant component. Starting at 70nm semiconductor technology, leakage power will contribute with 50% to total circuit's power (Pant, De & Chstterjee, 1997).

As technology scales down to 32nm and below, the bulk CMOS technology has reaching the scaling limit. This scaling limit is due to exponential increase of leakage power, the increased short-channel effects, severe process variations, high power density etc. To overcome this scaling limit, various types of materials have been experiment by the researchers. Among these alternative devices MOSFET-like CNTFET device has been evaluated as one of the hopeful replacements in the nanoscale electronics. The reason that makes CNTFET is a promising device is that, it is compatible with high dielectric constant materials, a unique 1-D band-structure that restrains back-scattering and makes near-ballistic operation. Using the CNTFET, a high-k gate oxide can be deployed for lower leakage currents while keeping the on-current drive capability with MOSFET. CNTFET has lower short-channel effect, hence low Off-current and a higher sub-threshold slope than Si-MOSFET (Akturk, Pennington, Goldsman, & Wickenden, 2007).