

# Optimization Trends for Wireless Network On-Chip: A Survey

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## ABSTRACT

Designing sustainable and high-performance wireless multi-core chips requires a matchless tradeoff between many aspects including scalable and reliable architectures implementation which in its turn implies aware-wideband energy-efficient wireless interfaces and adopting innovative straightforward optimization approaches to achieve the optimal configuration with a minimal cost. This paper focuses on investigating various existing designs and methodologies for wireless network on chip (WiNoC) architectures, as well as the different emerging technologies and optimization tools for the design of a robust and reliable WiNoC infrastructure with a special focus on combinatorial optimization meta-heuristics.

## KEYWORDS

Meta-Heuristics, Multi-Core On-Chip, Optimization, Performance, Reliability, Scalability, WiNoC, Wireless Interface

## 1. INTRODUCTION

The need for a continuing progress in Network-on-Chips (NoC) design was being unimpaired so as to keep pace with the ever increasing in system-level integration, applications requirements in terms of high computing capabilities and QoS and the emerging of the next-generation information and communication technologies.

According to authors (Pande et al, 2009a) and (Ganguly et al, 2010), the traditional NoC paradigm has encountered a serious issue regarding the communication performance (throughput and latency) and power consumption which impedes the system's development due to the planar metal interconnects.

A promising solution is to combine between traditional wired links for regular transmissions and express wireless paths for long distance communications to prevent multi-hop network delays. The WiNoC has emerged as a promising alternative for the conventional metallic interconnects based NoC and has been readily accepted to mitigate the large delay and high power dissipation issues offered by the NoC.

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In this paper, we will target the wireless solution, which consists in reducing the number of hops in a transmission path by placing wireless equipment on particular positions, and therefore, the message travels through smaller number of wireless nodes.

Although the on-Chip wireless-network can improve the performance more than any traditional NoC system, the presence of the additional wireless equipment leads to the imposition of hardware overhead.

Another important matter is the implementation of potential WiNoC architectures encompassing suitable topologies, routing schemes and arbitration techniques that matches well the application needs (Rahaman et al, 2016).

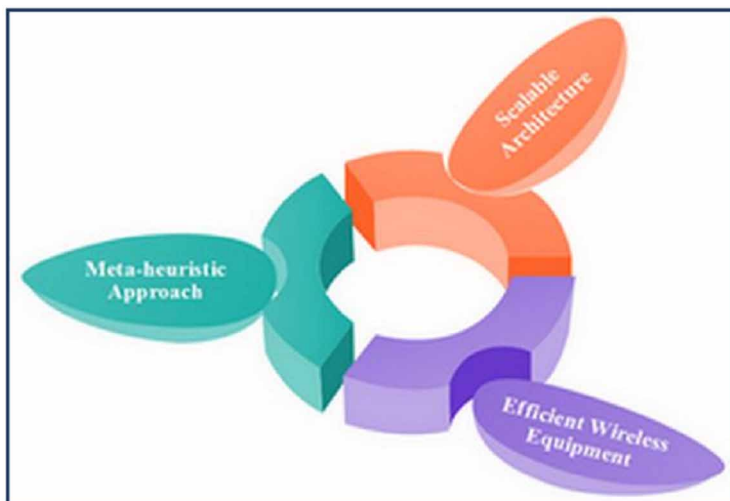
Numerous approaches have been developed in this context with the aim of pruning WiNoC systems. They resemble each other much more closely in conflicting objectives optimization while differ in the methodology. Generally, the potential solution can fall within one or a combination of the following three axes:

- Implementation of an aware wideband adaptive antenna, energy efficient transceiver often compatible nanometer Complementary Metal-Oxide Semiconductor (CMOS) technology.
- Application of meta-heuristic approaches for achieving the optimal hybrid/wireless configuration.
- Building a scalable architecture implying effective routing algorithm, innovative techniques and tools which ensure best reliability and cover all the wireless communication problems.

The most relevant WiNoC studies have stated that building a scalable and a reliable architecture with energy-efficient transceivers and a multi-objective optimized solution is not trivial. Since these criteria are conflict with each other, this may sometimes lead to unacceptable results on performance, and therefore, a deep multi-field study is inevitable.

Unlike the majority of the produced surveys (Li, 2012) (Deb and Mondal, 2014), (Marjan et al, 2017), (Ben Achballah et al., 2017), (KARIM et al., 2019), and (Lallas, 2019), our survey concentrates on studying wireless NoC infrastructures according to the three above mentioned axes with a focus on their additive design procedures introduced at Wireless Interface (WI) level, topologies and optimization meta-heuristics. Our objective is to study, compare and analyze the different results obtained from the released works in the context of WiNoC (Figure 1).

Figure 1. WiNoC study axes



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