

Chapter 15

SRAM Memory Testing Methods and Analysis: An Approach for Traditional Test Algorithms to ML Models

M. Parvathi

BVRIT HYDERABAD College of Engineering for Women, India

ABSTRACT

In the scenario of growing technologies towards single digit nanometer range, the existing algorithmic contemporary test methods have become inadequate in detecting all the faults within the static random access memory. To address the issues related to contemporary test methods, machine learning-based test analysis is proposed, which elevates the method of dataset preparation using various process parameters that are drawn from functional fault models (FFMs). The outcome of this proposed work is modeling of FFMs using ML regression, classification, and further prediction with accuracy analysis. The experiments resulted that logistic regression is best suited model that resulting with high accuracy in the range of 95% to 97%, compared to the linear regression model that results in accuracy levels in the range of 26.58% to 63%.

1. INTRODUCTION

Generally, IC testing comprises two ways: one is at the wafer level, and the other is at the package level. The wafer level test is a die or probe test that involves measurement of resistance and capacitance at the test location. If the observations differ from what was expected, this leads to fault identification. Similarly, the final test, which is the wafer test, will be done after packaging. This requires a probe, probe card, and test socket as a setup that decides whether the packaged chip has any faults or not. Deploying AI and machine learning (ML) algorithmic techniques in the VLSI domain at the design and manufacturing levels will reduce the test time. Most importantly, using automated learning algorithms will result in less effort in understanding and processing data at various abstraction levels. As a result, it reduces

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the manufacturing turnaround time, cost and further leads to an improvement in the IC yield. In general, defects in the IC layout will cause an effective fault in the circuit at the functional level. Machine learning helps while working with EDA tools in obtaining fault-free VLSI designs by predicting the defects on the chip and using that result to find better solutions during production.

A fault in embedded SRAM is an abstraction of a physical defect at various levels. Memory test algorithms are essential tools for detecting memory failures. Various test methods are used to detect and locate the fault (Shibaji Banerjee, Dipanwita Roy Chowdhury and Bhargab B. Bhattacharya (2005), TM Mak, Debika Bhattacharya, Cheryl Prunty, Bob Roeder, Nermine Ramadan, Joel Ferguson, Jianlin Yu. (1998), J. van de Goor. (1998), J.F. Li, K.L. Cheng, C.T. Huang, and C.W. Wu. (2001), Verilog Digital System Desigh. (2008)). March tests are one of the most efficient approaches for ensuring the correctness of SRAM functionality Balwinder Singh, Sukhleen Bindra Narang, and Arun Khosla. (2010). March tests are examples of algorithmic implementation that often target a definite fault model (Aiman Zakwan Jidin, Razaidi Hussin, Lee Weng Fook, Mohd Syafiq Mispan. (2021), Muddapu Parvathi, N. Vasantha, K. Satya Parasad (2012), Nor Azura Zakaria, W.Z.W. Hasan, I.A. Halin, R.M Sidek, Xiaoqing Wen. (2012)). Faults in SRAM may be single or multiple. Single faults are simple in nature, appear with the cell itself, and are easily captured by applying their corresponding fault models. However, multiple faults are not that simple to extract. Multiple faults are of two types: linked and unlinked. In linked faults, a fault in one cell will change the behavior of the other cell, whereas in unlinked faults, a change in the behavior of one cell does not affect the behavior of the other cell (Said Hamdioui, Ad J. van de Goor, Mike Rodgers. (2002), Rob Dekker, Frans Beenker, And Loek Thijssen. (1990)). There are many March algorithm models that can be observed in the literature that address single-stick and transition faults (G. Harutunyan And V. A. Vardanian, Y. Zorian. (2007), TM Mak, Debika Bhattacharya, Cheryl Prunty, Bob Roeder, Nermine Ramadan, Joel Ferguson, Jianlin Yu. (1998), M. I. Masnita, W. H. W. Zuha, R. M. Sidek, and A.H. Izhal (n.d)). However, as the process technology has grown to nanometer design techniques, SRAMs are brought to the level of sub-threshold operation, and the occurrence of multiple faults has grown in a similar manner, leading to the identification of a new type of March test to detect multiple faults (Chen-Wei Lin, Hung-Hsin Chen, Hao-Yu Yang, Chin-Yuan Huang, Mango C.-T. Chao, and Rei-Fu Huang. (2013). The other way of differentiating types of faults lies in its operation while detecting them. This gives the category of two types: static and dynamic faults. If the faults are sensitized by performing a single operation, they are called static faults, whereas if more than two operations are required, they are called dynamic faults (G. Harutunyan And V. A. Vardanian, Y. Zorian (2007). In this scenario, March primitives have become an essential measure of test models, in which faults can be observed by selecting appropriate sensitizing input and reading the corresponding output from the cell. Numerous March algorithms can be explored in the literature (Said Hamdioui, Zaid Al-Ars Ad J. van de Goor Mike Rodgers. (2003), A. Benso, A. Bosio, S. Di Carlo, G. Di Natale, P. Prinetto. (2006), Bosio A., Di Carlo S., Di Natale G., Prinetto P. (2007), Alberto Bosio, Giorgio Di Natale. (2008), Aiman Zakwan Jidin, Razaidi Hussin, Lee Weng Fook, Mohd Syafiq Mispan, Nor Azura Zakaria, Loh Wan Ying, and Norshuhani Zamin (2022), Aiman Zakwan Jidin, Razaidi Hussin, Mohd Syafiq Mispan, Lee Weng Fook, Loh Wan Ying (2022), G. Nguyen et al. (2019), C. Shorten and T. M. Khoshgoftaar (2019), R. Vinayakumar, M. Alazab, K. P. Soman, P. Poornachandran, A. Al-Nemrat, and S. Venkatraman (2019), K. Sivaraman, R. M. V. Krishnan, B. Sundarraj, and S. Sri Gowthem (2019), A. D. Dwivedi, G. Srivastava, S. Dhar, and R. Singh (2019), F. Al-Turjman, H. Zahmatkesh, and L. Mostarda (2019), S. Kumar and M. Singh (2019), L. M. Ang, K. P. Seng, G. K. Ijamaru, and A. M. Zungeru (2019), B. P. L. Lau et al. (2019), S. Martirosyan and G. Harutyunyan (2019), A. J. Van De Goor (1993), N. A. Zakaria (2013), I.S. Irobi, Z.

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