

Chapter 1

Electronic Hardware for Fuzzy Computation

Koldo Basterretxea

Universidad del País Vasco/Euskal Herriko Unibertsitatea (UPV/EHU), Spain

Inés del Campo

Universidad del País Vasco/Euskal Herriko Unibertsitatea (UPV/EHU), Spain

ABSTRACT

This chapter describes two decades of evolution of electronic hardware for fuzzy computing, and discusses the new trends and challenges that are currently being faced in this field. Firstly the authors analyze the main design approaches performed since first fuzzy chip designs were published and until the consolidation of reconfigurable hardware: the digital approach and the analog approach. Secondly, the evolution of fuzzy hardware based on reconfigurable devices, from traditional field programmable gate arrays to complex system-on-programmable chip solutions, is described and its relationship with the scalability issue is explained. The reconfigurable approach is completed by analyzing a cutting edge design methodology known as dynamic partial reconfiguration and by reviewing some evolvable fuzzy hardware designs. Lastly, regarding fuzzy data-mining processing, the main proposals to speed up data-mining workloads are presented: multiprocessor architectures, reconfigurable hardware, and high performance reconfigurable computing.

INTRODUCTION

Electronic hardware development for fuzzy inference-based computing systems (fuzzy hardware) has been an active research area almost since the first papers on successful fuzzy logic applications, mainly fuzzy controllers, were published in the early eighties. Although historically, due to the greater flexibility and compatibility, as well as the advantages and easiness of using high level languages, the majority of fuzzy inference system (FIS) implementations have been software developments to be run on general purpose processors (GPP), only concurrent computation architectures with specific processing units

DOI: 10.4018/978-1-60566-858-1.ch001

can take greatest advantage of fuzzy computation schemes. The development of fuzzy hardware has been mainly motivated by real-time operation demands, or by low power and/or small area occupation requirements. In this sense, the first fuzzy hardware researchers basically tried to design fuzzy chips capable of processing fuzzy control laws in a more efficient manner in terms of processing speed, occupied area and consumed power. But not only is computing efficiency a concern for fuzzy hardware designers; system programmability, compatibility of input/output signals and scalability at various levels (word-length, partition of the input and output domains, number of rules, or overall throughput gain) are also important features to be considered.

Design of fuzzy hardware is strongly conditioned by the target application it is addressed to. In consequence, many different application-specific designs have been reported, each of them showing characteristic features, strengths and weaknesses. The choice of the development platform and implementation technology is closely linked with this issue, and may itself bias the obtainable final features. Despite this, implementation of a general purpose fuzzy ASIC (Application Specific Integrated Circuit) suitable for any fuzzy rule-based application has been somehow sought but never achieved by fuzzy hardware designers, both in academic and in commercial contexts. It has been the arrival of high capacity reconfigurable hardware and the drastic changes in the design processes of complex digital systems associated with this technology that has finally made obsolete the general purpose fuzzy hardware objective. Last generation reconfigurable hardware platforms allow the implementation of optimized complex hardware/software codesigned adaptive and on-the-fly reconfigurable systems for application specific computation. The combination of reconfigurable hardware with the use of standardized hardware description languages (HDL) has entailed the transference of the task of achieving desirable features such as flexibility, scalability, reusability, etc from the hardware itself to the description or modeling of this hardware.

Fuzzy data management and analysis methods do not rest normally on a rule-based inference scheme, so the development of hardware for fuzzy data-mining has usually little to do with what is referred to as “fuzzy hardware”. In fact, fuzzy data-mining algorithms have been traditionally implemented by software applications running on GPPs, since there were not usually tight requirements for computation time, occupied silicon area or consumed power. On the contrary, flexibility, scalability and good interaction with data base storage systems were the only concerns. Nonetheless, nowadays, due to the increasing complexity of data-mining algorithms and the growing amount of data to be processed by them, sometimes with time constraints, more attention is being paid to the hardware acceleration of this kind of application. This field can be considered, together with scientific computation, a natural target for high performance computing (HPC). Consequently, specific hardware development for parallel processing or coprocessing of data-mining algorithms has been gaining relevance in recent years.

The chapter is organized as follows: Section 2 introduces the main hardware implementation variants performed since first fuzzy hardware chips were published and until the consolidation of reconfigurable hardware for complex digital system implementation. First of all, the distinctive characteristics of fuzzy inference-based computation that pushed researchers to find specifically designed hardware are described. Secondly we summarize the general pros and cons of the two main design approaches used for fuzzy hardware realizations, the digital approach and the analog approach; the performance indexes used for fuzzy hardware characterization are also briefly discussed. The bulk of the section follows by analyzing the different solutions proposed by hardware designers both for digital and analog approaches in a taxonomical way, giving examples of the most representative publications in the area. In Section 3 the evolution of fuzzy hardware implementations based on reconfigurable hardware and its relationship

28 more pages are available in the full version of this document, which may be purchased using the "Add to Cart" button on the publisher's webpage:
www.igi-global.com/chapter/electronic-hardware-fuzzy-computation/38563

Related Content

Artificial Insect Algorithms for Routing in Wireless Sensor Systems

Li-Minn Ang, Adamu Murtala Zungeru, Kah Phooi Seng and Daryoush Habibi (2015). *Emerging Research on Swarm Intelligence and Algorithm Optimization* (pp. 191-213).

www.irma-international.org/chapter/artificial-insect-algorithms-for-routing-in-wireless-sensor-systems/115305

Hybrid Linear Search, Genetic Algorithms, and Simulated Annealing for Fuzzy Non-Linear Industrial Production Planning Problems

P. Vasant (2013). *Meta-Heuristics Optimization Algorithms in Engineering, Business, Economics, and Finance* (pp. 87-109).

www.irma-international.org/chapter/hybrid-linear-search-genetic-algorithms/69882

An Efficient Constructive Heuristic for the Cutting Stock Problem Applied in a Foam Mattress Industry

Mariem Baazaoui, Souhir Elleuch and Hichem Kamoun (2022). *International Journal of Applied Metaheuristic Computing* (pp. 1-20).

www.irma-international.org/article/an-efficient-constructive-heuristic-for-the-cutting-stock-problem-applied-in-a-foam-mattress-industry/298317

Issues Related to Acceleration of Algorithms

(2022). *Implementation of Machine Learning Algorithms Using Control-Flow and Dataflow Paradigms* (pp. 173-194).

www.irma-international.org/chapter/issues-related-to-acceleration-of-algorithms/299347

Comparative Performance Evaluation of Fractional Order PID Controller for Heat Flow System Using Evolutionary Algorithms

Rosy Pradhan and Bibhuti Bhusan Pati (2019). *International Journal of Applied Metaheuristic Computing* (pp. 68-90).

www.irma-international.org/article/comparative-performance-evaluation-of-fractional-order-pid-controller-for-heat-flow-system-using-evolutionary-algorithms/234688