Chapter 29
Green Semicondoctor Design Techniques and Challanges

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ABSTRACT

The large emission of Carbon dioxide (CO2) is not only affecting our ecology but also affecting human life. In schools, offices, factory and crowded railway/bus stations i.e crowded places with insufficient ventilations CO2 affects human life most. In a closed environment like school, If CO2 level starts raising above 700 parts per million (ppm) people will feel objectionable body odors and as it increase further people will feel very uncomfortable, dizzy and have headache etc. Our goal is to reduce CO2 emission and lower global warming. In Semiconductor Industry as the digital technology grows, the functionality of our electronics devices (For example: - Mobile phone, PC's, home appliances etc) is constantly improves and mean while the demand for electronic devices to be more environment friendly is increasing. So we have to design systems with Low power consumption to curtail down green house gas emission as well as low power design are also a requirement of today's market. The usage of mobile device in all kinds of applications is increasing day by day. These applications and corresponding devices also have their power requirements. The demand for mobile consumer device has made the power management the number one consideration in today's system design. To increase battery life, system chip designer needs to adopt an aggressive power management technique which includes multi voltage Design Island, power gating, dynamic voltage, frequency scaling, clock gating etc in the system. Adding all these greatly complicates the verification for the chip. Normally the designer neglects the implementation of power saving techniques due to the tradeoff between power reduction and verification costs. The costs become

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more important in terms of business, which leads to more power consumption. Those details can still be implemented provided we use right kind of tools & techniques that are also combined with design experience. In this chapter the focus is to firstly describe low power design techniques, its verification challenges and its solutions followed by the case study. It also guides for the selection of programmable device & RTL Core design criteria. To make green electronics devices we have to design system with low power design techniques.

OVERVIEW

To build environment friendly electronics devices low power design techniques have vast application and scope in coming era, low power designs are going to dominate not only electronics world but all product design sectors. To build digital low power systems we have to start planning at the Register transfer level (RTL) coding itself, for saving power at Register transfer level (RTL) use below mentioned techniques, you can find more details about these techniques in references section provided on last page of this chapter.

- Early Power estimation. (www.xilinx.com, www.fijutsu.com)
- Multi power source design technology reduces power consumption while active. (Mayo, N. & Ranganathan, P., 2005)
- Combinational clock gating reduces power consummation while idle.
- Sequential clock gating reduces power consumption while idle.

EARLY POWER ESTIMATION

Early power estimation is always the preferred one because if after finishing the system design we founding that system is exceeding power budget then all money and efforts put on designing that system will be waste. That's why always do power estimation before starting the design. Now question is how we can do early power estimation or how can we define power consumption threshold limit for a System on chip (SOC) targeted for ASIC or FPGA? It is possible to calculate approximate power consumption number for both ASIC and FPGA targeted System on chip (SOC) designs at design architecture stage. The estimated power will help us in defining thresholds limits for power utilization by SOC. For ASIC rough estimation of gate count (Approximate digital gate count, Power requirement of analog blocks and other ready to use IP cores) and power calculation parameter provided by target technology vendor will be utilized to calculate approximate power consumption for ASIC targeted SOC. Early power estimation for FPGA is similar to ASIC but here life is bit easy and which gives us lots of choice in selection of target FPGA device, most of FPGA vendors use to provide power calculation excel sheets (For example Xilinx, we can go to www.xilinx.com and download early power estimation excel sheets free of costs) where we have to enter rough estimation of gate count numbers like in case of ASIC and select targeted FPGA device which meets basic requirements like which meets frequency and silicon size requirement of our SOC. By using early power estimation excel sheets of different vendor not only we will do approximate power estimation of our SOC but after comparing their results we can finalize a FPGA device which is also a cost effective solution for our SOC. Now the question is how early power estimation will help us in designing a low power solution? After doing early power estimation of our SOC architecture we know two very important points one how far we are from boundaries of our power budget, second our SOC architecture is a feasible solution or not in terms of cost and power requirements market is excepting. Once we know these two things and