Chapter 19 Multi-Core Embedded Systems

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ABSTRACT

Multiple processors, microcontrollers, or DSPs have been used in embedded systems to distribute control and data flow according to the application at hand. The recent trends of incorporating multiple cores in the same chip significantly expands the processing power of such heterogeneous systems. However, these trends demand new ways of building and programming embedded systems in order to control cost and complexity. In this context, the authors present an overview on multi-core architectures and their intercore communication mechanisms, dedicated cores used as accelerators, and hardware reconfiguration providing flexibility on today's multi-core embedded systems. Finally, they highlight tools, frameworks, and techniques for programming multi-cores and accelerators in order to take advantage of their performance in a robust and cost effective manner.

1. INTRODUCTION

Embedded systems comprise diverse devices, ranging from consumer multimedia devices to industrial controllers. These systems are designed to perform specific tasks with high reliability requirements, low power consumption, real-time response demands, functional flexibility and low cost. In the case of multimedia processing and high-speed telecommunications, the real-time constraints and quality of service demanded require intensive computation capabilities and careful system design.

Multiprocessor architectures have become the foundation of most common appliances, such as digital TV, navigation systems and wireless devices. During the last four decades the drive for performance has resulted in microprocessors becoming faster, clocked at higher-frequencies, and having a more complex architecture. Individual processors that integrate many processing elements in the same chip have recently become mainstream, spreading to embedded systems with advanced performance requirements. Apart from being an opportunity to use more processing power for demanding applications, distributing computations on many processors also addresses the problem of power dissipation, which is critical for small embedded systems that run on batteries or other limited power sources.

The transition from the single processor (*uniprocessor*) to the multi-core as a component for building embedded systems means that system design and building must adapt. Current system building techniques must be updated and new ones must be developed to match the new hardware capabilities.

This chapter aims at giving an overview of the current state of incorporating multi-cores into embedded systems. We give the basic background (Section 2) needed for understanding embedded multi-cores at the hardware level and from the programmer's view. We describe (Section 3) the main changes that they bring to embedded systems design and the issues that arise, followed by the practices and tools that researchers and the industry have found effective in addressing these problems. We then give an overview of the emerging trends related to embedded multi-cores in Section 4 and we conclude in the last section.

2. BACKGROUND

In this section we describe the current state of multi-core hardware for embedded systems, both homogeneous and heterogeneous. We then proceed to give the basic elements of the programmer's view over multi-core hardware.

2.1. Multi-Core Hardware

Moore's law is an observation that has predicted hardware development for more than 40 years. It states that the number of transistors that can be placed on an integrated circuit roughly doubles every two years. This became the basis for the uniprocessor scaling of the 1970s-2000s, where the frequency of the chips increased by orders of magnitude, boosting performance and giving system designers headroom for building efficient systems on a decreasing budget.

Due to physical limitations related to heat dissipation and power consumption in high operating frequencies, it was recently realized (Kish, 2002) that current techniques for building integrated circuits cannot sustain frequency scaling. Since Moore's law still holds, the industry switched to placing more microprocessors, known as *cores*, into so-called *multi-core processors*, or *multicores*. Assuming that Moore's law will continue to hold, it is expected that the number of cores contained in a System-on-Chip (SoC) will double approximately every two years (Paulin, 2010).

The mainstream adoption of multi-cores has recently pushed such microprocessors inside embedded systems, promising to speed up computations and improve power consumption. Since embedded systems were already heterogeneous, using many custom processors in the same system, these new multi-cores, often integrated in a multiprocesor System-on-Chip (MPSoC), add an extra dimension to embedded system design, as homogeneous components in a heterogeneous environment.

Homogeneous multi-cores consist of the same processing element repeated on the die, to be used as a conventional symmetric multiprocessor. For example, the Tilera TILEPro64 processor (TILERA, n.d.) contains 64 identical interconnected cores targeting high-performance embedded applications with scalable performance, power efficiency, and low processing latency. The TMS320C6678 multi-core DSP from Texas Instruments (Texas Instruments, n.d.b) contains eight TMS320C66x DSP Core Subsystems, each with a C66x Fixed/Floating-Point core, shared memory and a network coprocessor. The Parallax Propeller chip contains eight processors that can operate simultaneously, either independently or 16 more pages are available in the full version of this document, which may be purchased using the "Add to Cart" button on the publisher's webpage: www.igi-global.com/chapter/multi-core-embedded-systems/76966

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